REMARKS

Reconsideration and allowance in view of the foregoing amendments and the following remarks are respectfully requested.

Claims 1-7 are pending in this application, claim 7 being new.

In the Official Action, the Examiner noted that Fig. 1 should be designated as "Prior Art". In a separate Drawing Change Authorization Request accompanying this Amendment, it has been respectfully requested that certain drawing changes indicated in red be approved for entry in this application. It is proposed that Fig. 1 be labelled as prior art and that Fig. 4 have descriptive matter removed and the individual waveforms labeled separately adjacent the vertical axis. The specification is amended herein at page 10, line 17, so as to add the descriptive matter removed from Fig. 4. It is respectfully requested that the proposed corrections be entered.

The specification was objected to under 37 C.F.R. § 1.75(d) for not specifically disclosing an AND circuit. Certainly the Examiner appreciates that those of any skill in the art know that an AND gate and an inverter form a NAND gate. Fig. 3 shows clearly a NAND gate 34 and an inverter 36 inverting the output thereof. Thus, Fig. 3 shows clearly an

AND circuit formed from NAND gate 34 and inverter 36. The specification is amended at page 9, line 33 herein to disclose explicitly that a NAND gate may be formed by the combination of an AND gate and an inverter, and that a NOR gate may be formed by the combination of an OR gate and an inverter.

The specification was objected to under 35 U.S.C. § 112, first paragraph, for allegedly failing to provide an enabling disclosure for claims 4-6, and claims 4-6 are rejected for the same reasons. The Applicant thanks the Examiner for the suggestion of two minor changes to claim 4 so as to overcome this objection and rejection. Claims 4-6 have been carefully reviewed and are amended appropriately herein so as to recite subject matter which is enabled fully by the disclosure. It is therefore respectfully requested that the objection and rejection be withdrawn.

Claims 1-6 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite, and claim 1 was objected to for a noted informality. The Applicant thanks the Examiner for the indication that claims 2 and 3 would be allowable if rewritten to overcome the section 112 rejection. Claims 1-6 have been carefully reviewed in light of the Examiner's comments and are amended appropriately herein so as to

be more definite. Claims 1-6 are now in conformance with 35 U.S.C. § 112. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1 and 4-6 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 5,329,168 to Sugibayashi et al. ("Sugibayashi"). The Applicant respectfully traverses the rejection.

Claims 1 and 4-6 recite a PMOS transistor and a MOS transistor having a gate connected to the negative voltage and having a channel connected in series with the first MOS transistor and between the power supply and a ground supply, the MOS transistor being operated in response to a level of the negative voltage.

Sugibayashi teaches a two-bias generator circuit which is selectively powered from either an internal power source or an external power source (Sugibayashi, col. 1, lines 8-12). A redundant substrate bias system is formed from a first bias voltage producing circuit 13c which biases the substrate 11 until a second bias voltage producing circuit 13d is powered with sufficient internal power voltage level Vint (Sugibayashi, col. 5, lines 23-27 and Figs. 4 and 6).

The Examiner alleges that Sugibayashi teaches, in Figs. 4 and 6, a controller (13a of Fig. 4, NR1 of Fig. 6) and a PMOS transistor Qp2 (Office Action at 4).

Sugibayashi teaches a PMOS transistor Qp2 in series with a second voltage divider connected between a reference voltage (not a power supply voltage as in the present invention) and the substrate (not a ground supply voltage as in the present application). Thus, Sugibayashi fails to teach or suggest a PMOS transistor as claimed by claims 1 and 4-6.

Moreover, the MOS transistor Qn1 taught by Sugibayashi is not in series with the PMOS transistor as claimed by claims 1 and 4-6.

According to the present invention, power is selectively applied to a substantially otherwise conventional substrate voltage level detector. A PMOS transistor 38 is controlled by a controller 28 to be turned **OFF** in accordance with an output of the controller 28. This prevents unnecessary consumption of electrical power through the substrate voltage level detector at times when such consumption of power is not necessary.

Sugibayashi fails to disclose, teach or suggest such power consumption techniques. Rather, Sugibayashi teaches a two-

bias generator circuit which is selectively powered from either an internal power source or an external power source (Sugibayashi, col. 1, lines 8-12).

Furthermore, claims 4-6 recite that the PMOS transistor selectively provides power to the MOS transistor in response to the output signal of the controller circuit.

Sugibayashi fails to disclose, teach or suggest a MOS transistor or a PMOS transistor as recited, much less a PMOS transistor which selectively provides power to a MOS transistor as claimed by claims 1 and 4-6.

For all the above reasons, claims 1 and 4-6 are patentable over the cited art. It is therefore respectfully requested that the rejection be withdrawn.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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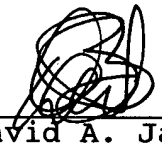
By  20817 for

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